Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (Currently Amended) A microelectronic structure, comprising:

a substrate comprising circuits;

a plurality of conductive bumps provided in adjacent relationship to each other on [said] the substrate in electrical contact with [said] the circuits, each of [said] the plurality of conductive bumps including an electrically insulative layer having an upper surface, a pair of sidewalls, an outer wall and an inner wall; and

a conductive layer provided [on] over the electrically insulative layer of each of [said] the plurality of conductive bumps,

wherein [said] the conductive layer is absent from at least one of [said] the sidewalls.

2. (Currently Amended) The microelectronic structure of claim 1, wherein [said] the conductive layer is absent from both of [said] the pair of sidewalls.

3. (Currently Amended) The microelectronic structure of claim 1, further comprising at least one shoulder provided in [said] the conductive layer at [said] the upper surface.

4. (Cancelled)

5. (Currently Amended) The microelectronic structure of claim 1, wherein [said] the conductive layer is absent from [said] the inner wall.

6. (Currently Amended) The microelectronic structure of claim 5, wherein [said] the conductive layer is absent from both of [said] the pair of sidewalls.

7. (Currently Amended) The microelectronic structure of claim 5, further comprising at least one shoulder provided in [said] the conductive layer at [said] the upper surface.

8. (Cancelled)

9. (Currently Amended) The microelectronic structure of claim 1, wherein [said] the conductive layer is formed of a conductive metal selected from the group consisting of Au, Ag, Pt, Pd, Al, Cu, Sn and alloys thereof.

10. (Currently Amended) The microelectronic structure of claim 9, wherein [said] the conductive layer is absent from both of [said] the pair of sidewalls.

11. (Currently Amended) The microelectronic structure of claim 9, further comprising at least one shoulder provided in [said] the conductive layer at [said] the upper surface.

12. (Cancelled)

13. (Currently Amended) A microelectronic structure, comprising:

a substrate comprising circuits;

a plurality of conductive bumps provided in adjacent relationship to each other in rows on [said] the substrate and in electrical contact with said circuits, each of [said] the plurality of conductive bumps including an electrically insulative layer having an upper surface, a pair of sidewalls, an outer wall and an inner wall;

a conductive layer provided [on] over the electrically insulative layer of each of [said] the plurality of conductive bumps, wherein [said] the conductive layer is absent from at least one of [said] the sidewalls; and

a protection layer provided on [said] the substrate adjacent to [said] the rows of [said] the plurality of conductive bumps.

14. (Currently Amended) The microelectronic structure of claim 13, wherein [said] the conductive layer is absent from both of [said] the pair of sidewalls.

15. (Currently Amended) The microelectronic structure of claim 13, wherein [said] the conductive layer is absent from [said] the inner wall.

16. (Currently Amended) The microelectronic structure of claim 13, further comprising a test probe pad provided on [said] the substrate adjacent to each of [said] the plurality of conductive bumps and in electrical contact with [said] the conductive layer.

17.-20. (Cancelled)

21. (New) A microelectronic structure, comprising:

a substrate;

a plurality of conductive bumps formed on the substrate, each of the plurality of conductive bumps including an electrically insulative layer having an upper surface and a side surface; and

a conductive layer formed over the electrically insulative layer of each of the plurality of conductive bumps exposing at least one portion of the side surface.

22. (New) The microelectronic structure of claim 21, wherein the conductive layer exposes at least one portion of the upper surface.

23. (New) The microelectronic structure of claim 21, wherein the plurality of conductive bumps are formed in rows in a staggered pattern one row to another.

24. (New) The microelectronic structure of claim 21, wherein the conductive layer exposes the portion of the side surface of the electrically insulative layer of at least one of the plurality of conductive bumps that faces a center of the substrate.

25. (New) The microelectronic structure of claim 21, wherein the conductive layer exposes at least one of the side surfaces of the electrically insulative layers of two immediately adjacent conductive bumps.

26. (New) The microelectronic structure of claim 21, wherein the conductive layer extends from the upper surface via a portion of the side surface to the substrate and extends further over the substrate.

27. (New) A semiconductor package, comprising:

a first substrate;

a plurality of conductive pads formed on the first substrate;

a microelectronic structure including:

a second substrate;

a plurality of conductive bumps formed on the substrate corresponding to the plurality of conductive pads, each of the plurality of conductive bumps including an electrically insulative layer having an upper surface and a side surface; and

a conductive layer formed over the electrically insulative layer of each of the plurality of conductive bumps exposing at least one portion of the side surface; and

a film disposed between the first substrate and the second substrate for electrically connecting the plurality of conductive bumps to the plurality of conductive pads.

28. (New) The semiconductor package of claim 27, wherein the conductive layer exposes at least one portion of the upper surface.

29. (New) The semiconductor package of claim 27, wherein the plurality of conductive bumps are formed in rows in a staggered pattern one row to another.

30. (New) The semiconductor package of claim 27, wherein the conductive layer exposes the portion of the side surface of the electrically insulative layer of at least one of the plurality of conductive bumps that faces a center of the substrate.

31. (New) The semiconductor package of claim 27, wherein the conductive layer exposes at least one of the side surfaces of the electrically insulative layers of two immediately adjacent conductive bumps.

32. (New) The semiconductor package of claim 27, wherein the conductive layer extends from the upper surface via a portion of the side surface to the substrate and extends further over the substrate.

33. (New) The semiconductor package of claim 27, wherein the film includes one of an anisotropic conducting film or a non-conductive film.

34. (New) The semiconductor package of claim 27, wherein the electrically insulative layer includes polyimide.